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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/424,966	03/06/2000	AKIHIDE SHIBATA	247322001700	8894

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EXAMINER

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ART UNIT

PAPER NUMBER

2811

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Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/424,966	SHIBATA ET AL.
Examiner	Art Unit	
Steven Loke	2811	

*-- The MAILING DATE of this communication appars on the cover sheet with the correspondence address --*

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 07 November 2001 .

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1-36 is/are pending in the application.

4a) Of the above claim(s) 4,5,7,9,11,13,15,17,19,21,23,25,27 and 29-36 is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1-3,6,8,14,22,24 and 28 is/are rejected.

7)  Claim(s) 10,12,16,18,20 and 26 is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)  The proposed drawing correction filed on \_\_\_\_\_ is: a)  approved b)  disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)  The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)  All b)  Some \* c)  None of:

1.  Certified copies of the priority documents have been received.
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14)  Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)  The translation of the foreign language provisional application has been received.

15)  Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3.  
4)  Interview Summary (PTO-413) Paper No(s). \_\_\_\_.  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_\_.

1. Claims 4, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29-36 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7.

2. Applicant's election without traverse of claims 1-3, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26 and 28 in Paper No. 7 is acknowledged.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The abstract is objected to because of the following informalities: In line 5 of the abstract, it is believed that the reference numeral of the gate insulating film is 6 instead of 8.

Appropriate correction is required.

6. Figures 22 and 23 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. Claims 22, 24 and 28 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification never discloses the drain terminals of the P-type semiconductor element and N-type semiconductor element are connected to each other to form an output terminal as claimed in claim 22.

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Merrill et al.

In regards to claim 1, Merrill et al. shows all the elements of the claimed invention in fig. 2. It comprises: a semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region [40a, 46a] having a source terminal

[S] and a drain region [42a, 44a] having a drain terminal [D] in a well [34a, 36a] formed in a semiconductor layer, and a gate terminal [G] fabricated on a channel region, formed between the source region and drain region, through a gate insulating film, wherein: each of the semiconductor elements is electrically separated from the others; and the well in each of the semiconductor elements is provided with a substrate terminal through a contact hole formed therein at a region [38a, 48a] other than the source region and drain region.

In regards to claim 2, it is inherent that the operating characteristics are changed by adjusting impurity concentration in the channel region and levels of a high voltage and a low voltage applied to the gate terminal and substrate terminal.

In regards to claim 3, the semiconductor layer in each of the semiconductor elements is electrically separated from each other by means of an oxide film [60c].

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al.

In regards to claim 1, Chang et al. discloses a CMOS in fig. 1I. It comprises: a semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region [26, 34] and a drain region [23, 32] in a well [8, 12] formed

in a semiconductor layer, and a gate terminal [20', 20"] fabricated on a channel region, formed between the source region and drain region, through a gate insulating film [16, 18], wherein: each of the semiconductor elements is electrically separated from the others; and the well in each of the semiconductor elements is provided with a substrate terminal contact hole formed therein at a region [28, 30] other than the source region and drain region.

It would have been obvious to have a source terminal, a drain terminal and a substrate terminal in each of the semiconductor elements because they provide electrical connection between the semiconductor element and the external circuit.

In regards to claim 2, it is inherent that the operating characteristics are changed by adjusting impurity concentration in the channel region and levels of a high voltage and a low voltage applied to the gate terminal and substrate terminal.

In regards to claim 3, it would have been obvious for the semiconductor layer in each of the semiconductor elements is electrically separated from each other by means of an oxide film because it is a conventional isolation material for integrated circuit.

12. Claims 6, 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. in view of Iwamatsu.

In regards to claim 6, Chang et al. differs from the claimed invention by not showing a high potential is supplied to a source terminal of the PMOS and a low potential is supplied to a source terminal of the NMOS, the gate terminals of the PMOS and NMOS are connected to each other to form a first input terminal, the substrate terminals of the PMOS and NMOS are connected to each other to form a second input terminal, and the

drain terminals of the PMOS and NMOS are connected to each other to form an output terminal.

Iwamatsu shows showing a high potential  $V_{DD}$  is supplied to a source terminal of the PMOS and a low potential is supplied to a source terminal of the NMOS, the gate terminals of the PMOS and NMOS are connected to each other to form a first input terminal  $V_{in}$ , the substrate terminals of the PMOS and NMOS are connected to each other to form a second input terminal when the clock voltages are 0 volt ( $CLK1=CLK2=0$  volt), and the drain terminals of the PMOS and NMOS are connected to each other to form an output terminal  $V_{out}$  in figs. 1-4.

Since both Chang et al. and Iwamatsu teach a CMOS device, it would have been obvious to have the circuit connection of Iwamatsu in Chang et al. because it is a conventional way to form a circuit in a semiconductor substrate.

In regards to claim 8, it would have been obvious to have the threshold voltage of claim 8 because it depends on the impurity concentrations of the wells and the voltage applied to the second input terminal.

In regards to claim 14, it would have been obvious to have the threshold voltage of claim 14 because it depends on the impurity concentrations of the wells and the voltage applied to the second input terminal.

13. Claims 10, 12, 16, 18, 20 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The first major difference in the claims not found in the prior art of record is a gate terminal of the P-type semiconductor element and a substrate terminal of the N-type semiconductor element are connected to each other to form a first input terminal, a gate terminal of the N-type semiconductor element and a substrate terminal of the P-type semiconductor element are connected to each other to form a second input terminal, and drain terminals of the P-type semiconductor element and N-type semiconductor element are connected to each other to form an output terminal. The second major difference in the claims not found in the prior art of record is a drain terminal of the N-type semiconductor element is supplied with a high potential and a drain terminal of the P-type semiconductor element is supplied with a low potential, the gate terminals of the P-type semiconductor element and N-type semiconductor element are connected to each other to form a first input terminal, the substrate terminals of the P-type semiconductor element and N-type semiconductor element are connected to each other to form a second input terminal, and the source terminals of the P-type semiconductor element and N-type semiconductor element are connected to each other to form an output terminal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers

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for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl

April 7, 2002.

Steven L. Loh  
U.S. Patent and Trademark Office

*Steven L. Loh*